

NON-PRIME PARAMETERS OF LDPC CODES WITH SYMMETRICAL SUB-MATRIX

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ABSTRACT

The performance of Low-density parity-check (LDPC) codes is based on the parity check matrix design. In this paper, the irregular symmetrical parity check matrix was designed using of non-prime number. Then the arbitrary block length can be obtained. The advantages of symmetrical matrix are: 1) easily and quickly design, 2) the good performance as good as random construction was obtained and 3) higher minimum distance, the higher error detection and correction ability was obtained. Moreover, the performance of designed non-prime parity check matrix is higher when compared with MAC and SC-Array. Our designed parity check matrix still has the general properties of LDPC codes.

Index Terms— LDPC Codes, non-prime, symmetrical, coding

1. INTRODUCTION

A Low Density Parity Check (LDPC) codes is error correcting codes which has code performance close to Shannon limit. This code has many advantages such as low error floor, high code rate, no cycle-4 and capability of detecting and correcting burst error. In this decade, many researches are concerning the LDPC codes performance development. A design of parity check matrix is one challenge of those researches, since of the performance of LDPC codes depends on the parity check matrix design. In the parity check matrix design, the sparse one's should be decreased but must be enough for data error correction. Richardson *et al.* [1] presented the LDPC codes construction algorithm to yield the performance very close Shannon limit with a difference of only 0.0045 dB. It has very high performance when used for long block length. Eleftheriou and Olcer [2] and Singhaudom *et al.* [3] proposed a parity check matrix structure for LDPC codes, using 'Cyclic Shift' construction. Their code performances are equivalence to the random parity check matrix structure LDPC codes. The performance test results show that the longer block length, the higher performance yielded.

LDPC Codes hold two types of parity check matrix: regular and irregular. For regular parity check matrix, Gallager [4] purposed a construction of a random parity check matrix

which has the same number of one element for every row and also has the same number of one element for every column, and without cycle-4. Fan [5] presented a design of an array parity check matrix structure. The complexity of parity check matrix construction is lower but still has the good performance as good as of the random parity check matrix. For irregular parity check matrix, because of its higher performance, when compared to a regular one, researchers are interesting on the later, e.g., [7], [2], [3] and [6]. In those works, the LDPC codes performances were improved by the variety of parity check matrix design. The complexity of the encoder can be made lower by using the triangular form matrices [2], [3] and [6].

In the design of parity check matrix of $jp \times kp$ sizes, the design parameters such as j , k and p should be suitably defined. Where j and k are integers, p is prime number and $j, k \leq p$. The traditional designs using of prime number parameter are presented in [4], [1], [5], [2], [3] and [6]. [4] has proposed the construction of regular LDPC codes with random parity check matrix and [1] have presented the evaluation of performance of this LDPC codes and the results shown that it performance close to the Shannon limit. [5] has proposed the array structure sub-matrix of parity check matrix with is modified from [4] and still be the regular LDPC codes for long block length. [2] have presented the modification of array structure sub-matrix from regular LDPC codes of [5] to be irregular using the concept of quasi-cyclic shift (α) into sub-matrix. [3] modified the parity check matrix from [2] by using interleave quasi-cyclic shift (ω). [6] have presented the parity check matrix for short and medium block lengths which is modified from [2] and [3].

For non-prime number sub-matrix constructions, this was firstly presented by Abematsu *et al.* [8] and followed by Chusin *et al.* [9]. Where, [8] modified the work proposed by [2] but with non-prime number construction parameters instead of prime number. Similarly [9] have modified the sub-matrix given by [3] and with non-prime number.

In this paper we propose a new design parity check matrix for arbitrary code length aims at improves the coding performance suitable for 4K bits block length using of symmetrical sub-matrix with non-prime number construction parameters. This paper is organized as follows: General perspective of LDPC codes is given in section II where

encoding and decoding are also included. Section III gives brief details of a symmetrical matrix. A design of parity check matrices for arbitrary and non-prime code lengths is outlined in section IV and the corresponding performance tests are reported in section V. Finally, the paper is concluded in section VI.

2. LDPC CODES

Low-density parity-check (LDPC) codes proposed by Gallager in 1962 [4], have attracted much attention given their good performance. The encoding and decoding of LDPC codes can be done by using of sparse parity check matrix H . The relationship between codeword bits and parity checks bit of the parity check matrix can be graphically presented by a Tanner graph [10]. A parity-check matrix H has n columns and m rows, and the codeword consists of n bits, which satisfy m checks, the number of message bits will be $k=m$, and the code rate is $R_c=k/n$. The number 1's in the parity check matrix in rows and columns represents an edge between the i -th bit node c_i and the j -th check node f_j .

For encoding of the LDPC codes, it is similar to other linear block codes, it has the relation;

$$C_{(1 \times n)} = \left[m_{(1 \times m)} \mid p_{(1 \times n-m)} \right] \quad (1)$$

where $p_{(1 \times n-m)}$ denotes the parity portion, and $m_{(1 \times m)}$ denotes the message portion respectively.

$$C_{(1 \times n)} H_{(n \times m)}^T = 0 \quad (2)$$

where C is a codeword matrix, and H is a parity check matrix. In a systematic form, C can be written as:

There are several methods for decoding the LDPC codes e.g.: Believe Propagation (BP), Sum-Product (SP), and Message Passing (MP). The Log-domain Sum-Product algorithm was used in this paper; it is the message passes between check nodes and bit nodes. In each pass the log likelihood ratio (LLR) is recorded for is probability of its likely symbol. By means of this method, the variable q_{ij} be the message sent from the i^{th} bit node to j^{th} check node along a connecting edge, and r_{ji} is the message sent from j^{th} check node to the i^{th} bit node along a connection edge. The message q_{ij} is computed based on the values sent from check nodes connecting to the i^{th} bit node excluding the j^{th} check node.

3. SYMMETRICAL MATRIX

A symmetrical matrix is a square matrix that is equal to its transpose matrix. Let A is a symmetrical matrix. Then

$$A = A^T \quad (3)$$

The entries of a symmetrical matrix are symmetric with respect to the main diagonal (top left to bottom right). So if the entries are written as $A = (a_{ij})$, then $a_{ij} = a_{ji}$. This also implies that

$$A^{-1} A^T = I, \quad (4)$$

where I is the identity matrix. The elements of a symmetric matrix A have the form:

$$A = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1n} \\ a_{12} & a_{22} & \cdots & a_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ a_{1n} & a_{2n} & \cdots & a_{nn} \end{bmatrix} \quad (5)$$

The parity check matrix based on the symmetrical matrix can easily be constructed and yields a good performance as same as randomly parity check matrix. It can be seen that the '1' elements in the constructed symmetrical parity check matrix is fairly well distributed. As a result, the higher value of the minimum distance is obtained. Consequently, the better error correction can be achieved. The code performance should be as good as, or similar to the random construction presented in [7].

4. DESIGN OF PARITY CHECK MATRICES

In this section, we detail the formulation of the H matrix by using the idea of symmetrical matrix instead of permutation. The new design symmetrical sub matrix is used to form H matrix in the same manner of the forming of array code proposed by [8].

4.1 Some Related Works

Fan [5] has introduced the array structure parity matrix that can offer comparable performance when compared to a random generated parity matrix reported by Gallager [4]. Other features: low noise floor and no existence of cycle-4, are kept as the original features of LDPC codes proposed in [4]. Fan's matrix is shown below.

$$H(p, j, k) \triangleq \begin{bmatrix} I & I & I & \cdots & I \\ I & \alpha & \alpha^2 & \cdots & \alpha^{k-1} \\ I & \alpha^2 & \alpha^4 & \cdots & \alpha^{2(k-1)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ I & \alpha^{j-1} & \alpha^{2(j-1)} & \cdots & \alpha^{(j-1)(k-1)} \end{bmatrix} \quad (6)$$

Where I is an identity matrix ($p \times p$),

α is a position permutation matrix ($p \times p$).

This yields the code rate of $R = 1 - \frac{pj-j+1}{p^2}$.

Eleftheriou and Ocler [2] have proposed the modified array codes (MAC) by applying cyclic shifting to Fan's array [5] given herewith in Eq. (7). The structure noted by Eq. (7) have the code rate of $R = 1 - (j/k)$. MAC offers superior performance to Fan's array as it can reduce number of "1" in the lower triangle. This leads to simpler encoder while preserving other LDPC's features.

$$H = \begin{bmatrix} I & I & \dots & I & I & \dots & \dots & I \\ 0 & I & \alpha & \dots & \alpha^{(j-2)} & \alpha^{(j-1)} & \dots & \alpha^{(k-2)} \\ 0 & 0 & I & \dots & \alpha^{2(j-3)} & \alpha^{2(j-2)} & \dots & \alpha^{2(k-3)} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & \dots & I & \alpha^{(j-1)} & \dots & \alpha^{(j-1)(k-1)} \end{bmatrix} \quad (7)$$

where I is an identity matrix ($p \times p$).

α is a position permutation matrix ($p \times p$).

Singhaudom *et al.* [3] have proposed the interleaved modified array LDPC developed base on the concept of [2] and named it as IMAC. By introducing the quasi cyclic matrix into the cyclic shifting the obtained matrix is given in Eq. (8). The identity matrix and the interleave matrix are shown in Eq. (9). The IMAC is superior to MAC when the block length is particularly long.

$$H = \begin{bmatrix} I & I & I\omega & I\omega^2 & I\omega^3 & \dots & I\omega^j \\ 0 & I & \alpha\omega & \alpha^2\omega^2 & \alpha^3\omega^3 & \dots & \alpha^{(k-2)}\omega^j \\ 0 & 0 & I & \alpha^2\omega^2 & \alpha^4\omega^3 & \dots & \alpha^{2(k-3)}\omega^j \\ \vdots & \vdots & \vdots & I & \alpha^3\omega^3 & \dots & \vdots \\ 0 & 0 & \dots & 0 & I & \dots & \alpha^{(j-1)}\omega^{(k-j)} \end{bmatrix}_{(jp \times kp)} \quad (8)$$

Where ω is the quasi cyclic matrix that constructed from identity matrix by cyclically-shifting of the matrix, I , i.e. $\omega^{n-1} = I$.

$$I = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}_{(5 \times 5)} \quad \text{and} \quad \omega = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}_{(5 \times 5)} \quad (9)$$

Abematsu *et al.* [8] have proposed the Size Compatible (SC)-Array LDPC Codes of which the parity check matrix shown in Eq. (10). The design can support arbitrary code lengths while achieving good error rate performance; it contains few or no cycle-4. It should be noted that [8] has used non-prime sub-block while [5] has. For the SC-array LDPC code, the permutation sub-matrix is decided to eliminate all cycle-4. Such a proposed cyclic shift $P_{sc}(j,k)$ is expressed by Eq. (11).

$$H = \begin{bmatrix} I & I & \dots & \dots & I & \dots & I \\ \alpha^{P_{sc}(2,k)} & I & \dots & \dots & \alpha^{P_{sc}(2,j)} & \dots & \alpha^{P_{sc}(2,k-1)} \\ \alpha^{P_{sc}(3,k)} & \alpha^{P_{sc}(3,k-1)} & I & \dots & \alpha^{P_{sc}(3,j)} & \dots & \alpha^{P_{sc}(3,k-2)} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \dots & \vdots \\ \alpha^{P_{sc}(j,k)} & \alpha^{P_{sc}(j,k-1)} & \dots & \dots & I & \dots & \alpha^{P_{sc}(j,k-j+1)} \end{bmatrix} \quad (10)$$

where

$$P_{sc}(j,k) = (j-1)(k-1) + \left\lfloor \frac{(j-1)(k-1)}{L} \right\rfloor \quad (11)$$

The IMAC cannot support the arbitrary code lengths, since the code length is restricted to be a multiple of prime number. Chusin *et al.* [9] have presented a design of parity check matrix to address this problem. Their design is based on the construction rows that don't have the same sub-matrix in the same row. They have shown that, with non-prime number, they achieved the same error rate performance as the prime sub-matrix size of IMAC in AWGN channels. The performance for long block lengths is also better when compared with [8].

4.2 LDPC Codes with Symmetrical Sub-matrix

We designed the H matrix by using of symmetrical matrix shown in Eq. (12) instead of permutation matrix. The symmetrical matrix S is of dimension $q \times q$ where q could be either prime or non-prime number. For the designed matrix size $q \times q$, let's define the binary element of matrix be $s_{xy} = \{0,1\}$ and the index r is bound to $r = (q/3) \times 2$. x and y are row and column indices respectively.

In designing of S matrix, the row elements can be computed as given by a pseudo code below:

```

Odd number row:
    bb=0; aa=0; x=1;
For cc=1 to q
    (row)
    for dd=1 to q
        (column)
        if ((2*q)-dd)-(2*bb)=dd then
s=1; goto 10;
    else
s=0
    end;
        end;
10:    cc=cc+2; bb=bb+1;
    if cc = ((2*q)-cc)-(2*bb) then
        goto 20;
        end;
20: end

```

The odd number columns can be generated by the transposition of obtained odd number rows as $S_{y,x} = (S_{x,y})^T$.

The construction or even number (2, 4, 6, ...) row and column of sub-matrix, S is to generate '1' at the $x=y$ position of each column. If there is no the '1', add this position with the '1', otherwise adding the '0'.

The resulted matrix is shown in Eq. (12);

$$S = \begin{bmatrix} 0 & 0 & 0 & 0 & \dots & 0 & 0 & 0 & \dots & 0 & s_{i,j} \\ 0 & s_{2,2} & 0 & 0 & \dots & 0 & 0 & 0 & \dots & 0 & 0 \\ 0 & 0 & 0 & 0 & \dots & 0 & 0 & 0 & \dots & s_{(x+2),(y-1)} & 0 \\ 0 & 0 & 0 & s_{4,4} & \dots & 0 & 0 & 0 & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \ddots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & s_{r,r} & 0 & 0 & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & 0 & 0 & \vdots & \vdots & \vdots \\ 0 & 0 & s_{(y-1),(x+2)} & \vdots & \vdots & \vdots & s_{(r+2),(r-1)} & \vdots & \vdots & \vdots & \vdots \\ s_{y,x} & 0 & 0 & 0 & \dots & \dots & 0 & 0 & \dots & 0 & 0 \end{bmatrix} \quad (12)$$

The example designed matrix of which $q=10$ is shown in Eq. (13).

$$S = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (13)$$

As shown in Eq. (13), it can be seen that the matrix hold transpose property or $S^T = S$ and there is not cycles 4 in sub-matrix. We then construct one time shifting or S^1 by performing cyclically-right shifting of the original S . The obtained matrix is given in Eq. (14).

$$S^1 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (14)$$

Other degree shifting can be performed similarly. The block shifting scheme is arranged similar to that proposed by [8]. Finally, the parity check matrix can be generated as given in Eq. (15). We use this formulation in code design for performance evaluation. In this design, three important parameters consist of j , k and L ($j, k \leq q$). Where j and k are integers and q is non-prime number of sub-matrix size.

$$H = \begin{bmatrix} I & I & I & I & \dots & \dots & I \\ 0 & I & \lambda^{(2,3)} & \dots & \lambda^{(2,j)} & \dots & \lambda^{(2,k-1)} \\ 0 & 0 & I & \lambda^{(3,4)} & \lambda^{(3,j)} & \dots & \lambda^{(3,k-2)} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \dots & \vdots \\ 0 & 0 & \dots & \dots & I & \dots & \lambda^{(j,k-j+1)} \end{bmatrix} \quad (15)$$

where

$$\lambda^{(j,k)} = S^{P_T(j,k)} \quad \text{and,}$$

$$P_T(j,k) = (j-1)(k-1) + \left| \frac{(j-1)(k-j)}{q} \right|$$

5. PERFORMANCE EVALUATION

The performance of our constructed parity check matrix was investigated for 4K bits blocks length. This is actually useful in the application of magnetic recording system where the sector size is 512 bytes. To compare with some exist publication the sub-matrix size of 68 is used. The test parameters are shown in Table I as below with iteration number of 30. The minimum distance of available published work was determined at $d_{min} = 336$ [2]. Our work has $d_{min} = 341$. This implies that our work should have higher capability of error detection and correction.

TABLE I: PARAMETERS FOR 4KBIT BLOCK SIZE

	j	k	q	R	Block size (bit)
MAC [2]	5	61	67	0.918	4087
SC-Array[8]	5	60	68	0.917	4080
This paper	5	60	68	0.917	4080

The design code is run for 30 iterations to the random-generated input sequence as also performed by MAC and SC-array. The obtained performance is shown in Fig. 1 below. The proposed code offers the same performance as MAC and SC-Array do. It only yields slightly better performance when E_b/N_0 is greater than 4.2 dB.

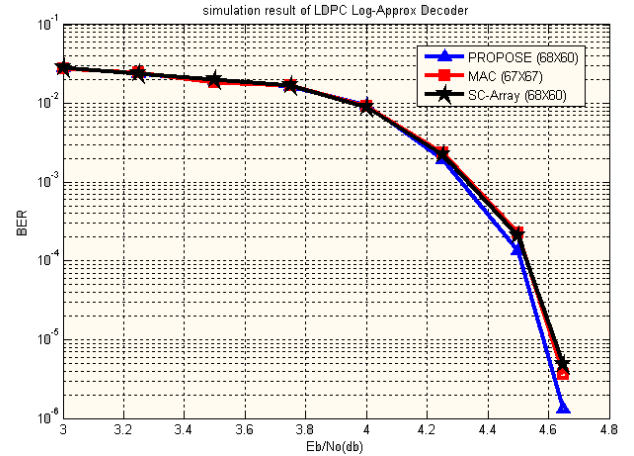


Fig. 1. The performance of proposed and existing LDPC codes (Iteration = 30)

The modified matrix proposed in this paper was also test for the block length of a particular size – say 4080, but at different sub-matrix size. This effect results in the changing of the code rate. We therefore intend for the code rate of better than 0.5. Parameters are given in Table II.

TABLE II: PERFORMANCE TEST PARAMETERS FOR EACH SUB-MATRIX SIZE

Block Size (bit)	j	k	q	R	Iterations
4080	5	60	68	0.917	30
4080	5	51	80	0.902	30
4048	5	44	92	0.886	30
4030	5	26	155	0.808	30
4063	5	17	239	0.706	30
4082	5	13	314	0.615	30
4100	5	10	410	0.5	30

Of the 30 iterations limit, the obtained result is shown in Fig. 2. It can be seen that the performance of the code can be improved when the sub-matrix size is increased as the sub-matrix size varies from 68 to 155. On the other hand, when the code rate is better than 0.8. However the decline in performance is observed when the sub-matrix size is more than 155. Therefore the good performance could be obtained only in particular range of sub-matrix size.

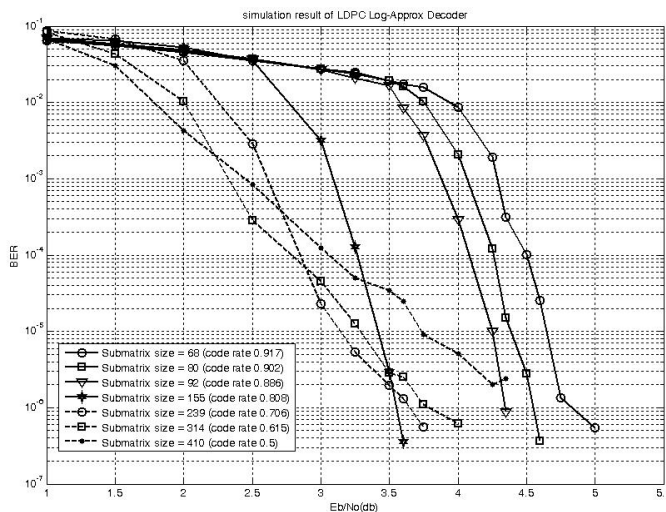


Fig. 2. The test results using different sub-matrix sizes (Iteration = 30)

6. CONCLUSIONS

The design of high-rate code with block sizes suitable for magnetic recording system is illustrated. The block size of the current application is about 4K bits. However, the actual size is determined based on particular data rate (Mbit/sec.) which practically optimized upon several parameters. To ease the design constrain we are trying to design a code that support any block size. The proposed parity check matrix is designed based on symmetrical property rather than permutation effort. Although the design code offers similar or slightly better performance compared to the published MAC [2] and SC-Array [8], the simulation shows that the size of sub-matrix affects the code performance. The larger sub-matrix leads to higher minimum distance and achieve the better performance than the smaller one. However, the sub-matrix size should less than 155, as discussed in the previous section. This proposed matrix still possesses suitable properties for magnetic recording system such as low-complexity encoding process, low error floor and capability of detecting and correcting burst errors.

In summary, the advantages of symmetrical matrix are: 1) easily and quickly design, 2) the good performance as good as random construction was obtained and 3) higher minimum distance, the higher error detection and correction ability was obtained. For future works, we plan to evaluate the performance to the 4Kbytes that using in the new generation of recording technology.

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