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# New Bias Voltage Generators for TFT-LCD's Drivers\*

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**SUMMARY** New positive and negative bias voltage generators for TFT-LCD's drivers utilizing charge pump circuits are introduced. The generators can generate positive or negative voltages with various amplitude by simply changing the number of pumping stages. By using the circuit simulation program HSPICE, it is demonstrated that the introduced generators can provide enough positive or negative voltages for TFT-LCD's drivers.

**key words:** TFT-LCD, charge pump circuit, voltage generator

## 1. Introduction

The dot inversion method for a TFT-LCD panel requires three driving signals ( $V_{sig}$ ,  $V_{COM}$  and  $V_G$ ) having several voltage levels as shown in Fig. 1. Accordingly, the PCB (Printed Circuit Board) to drive the TFT-LCD panel needs positive and negative bias voltages, such as  $\sim +5V$ ,  $\sim +10V$ ,  $\sim +23V$ ,  $\sim -5V$ ,  $\sim -10V$  and so on. Such bias voltages are generated by a DC-DC converter, and applied to the TFT-LCD panel through Y and X drivers as shown in Fig. 2. Usually, to obtain these bias voltages, we have been used DC-DC converters composed of capacitors, winding coils and amplifiers etc.,.

Important design objectives for the DC-DC converters in many applications include small size, low cost, and high efficiency etc.,. Small size and low cost can be obtained through a high level of integration and through design of coilless. The alternatives that do not require coils are linear regulators and switched-capacitor converters (also known as charge pumps). Especially, the switched-capacitor converters are widely used in integrated circuits where a voltage higher than or of opposite polarity to the input voltage is needed.

In this paper, we propose new positive and negative bias voltage generators for TFT-LCD's drivers

utilizing charge pump circuits [1], [2]. The generators allow a variety of bias voltages to be provided from a single power supply. The operating characteristics of the generators are also examined by using the circuit analysis program HSPICE in detail.

## 2. Circuit Configuration

To obtain large output current (more than several mA) by using only one charge pump circuit, we have to use large kick and control capacitors (more than several thousand pF) to drive the charge pump circuit. Also, size of MOS transistors composed of the circuit has to be large to reduce driving impedance. To avoid these problems, we propose new bias voltage generators composed of two charge pump circuits.

Figure 3 shows the schematic diagram of the proposed positive high-voltage generator with 10-stages to

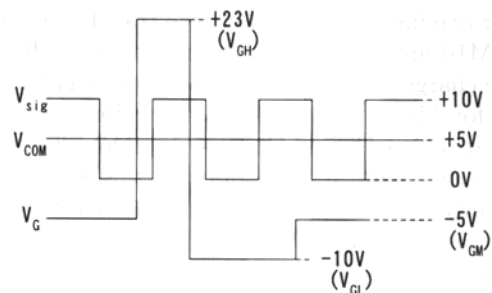


Fig. 1 Driving signals for TFT-LCD panel.

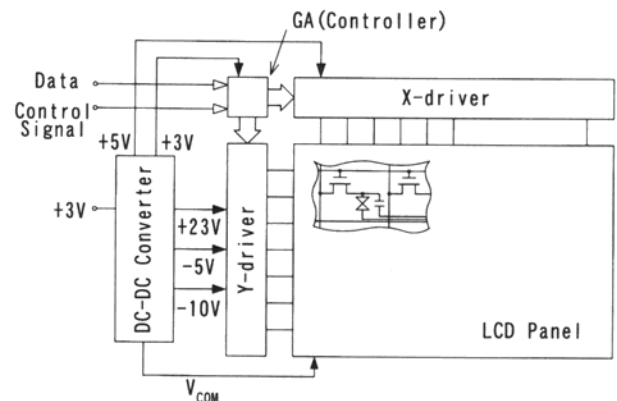


Fig. 2 Block diagram of TFT-LCD panel.

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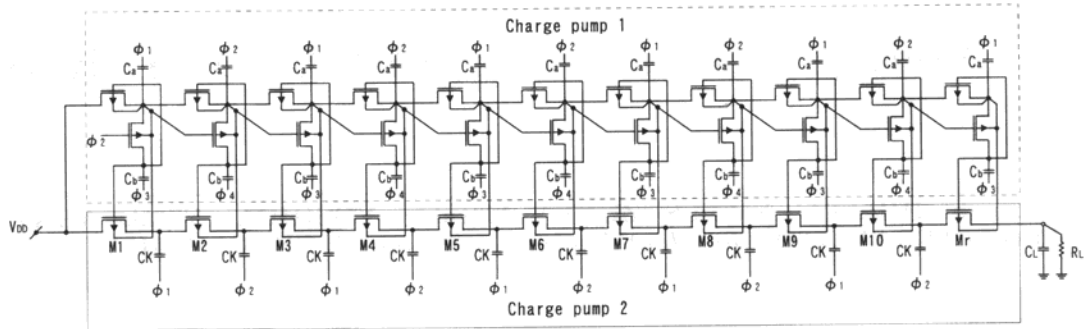


Fig. 3 Positive high-voltage generator.

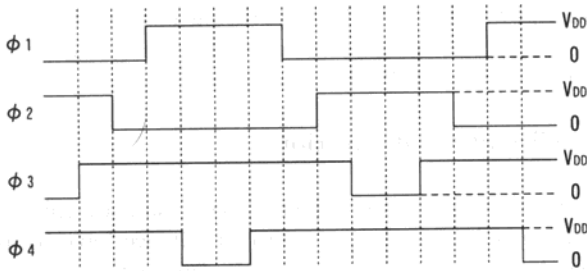


Fig. 4 Operating clock signals.

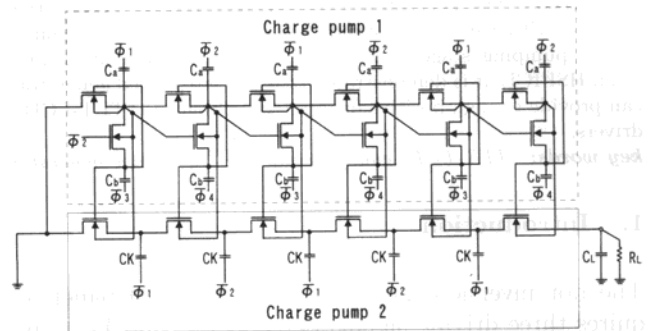


Fig. 5 Negative high-voltage generator.

get the high level gate signal  $V_{GH}$  (+23 V) of TFT. Also, Fig. 4 shows the operating clock signals  $\phi_1 \sim \phi_4$ , respectively. The clock signals have the voltage amplitude equal to the power supply voltage  $V_{DD}$ .

As can be seen in Fig. 3, the proposed generator consists of two charge pump circuits. Charge pump 1 is used for driving the gates of charge transfer transistors  $M1 \sim M10$  and a rectifying transistor  $M_r$ . That is to say, the charge pump 1 is only to generate gate control signals for  $M1 \sim M10$  and  $M_r$ . Therefore, the charge pump capacitors  $C_a$  and  $C_b$  have relatively small value. On the other hand, charge pump 2 that operates like the Dickson's charge pump [3] is to generate positive high-voltages for TFT-LCD's drivers. Therefore, the charge pump capacitors  $CK$  are larger than  $C_a$  and  $C_b$ .

In the charge pump 2, PMOS transistors  $M1 \sim M10$  and  $M_r$  driven by the charge pump 1 operate in non-saturation region. Therefore, the maximum output voltage  $V_o$  which can be generated by the generator with  $n$ -stages is approximately given by

$$V_o = (n + 1)(V_{DD} - V_{DS}) \quad (1)$$

where  $V_{DS}$  is drain-to-source voltage of  $M1 \sim M10$  and  $M_r$ . Also, the output current which can be delivered to the resistor  $R_L$  by this generator is determined by the value of the charge pump capacitors  $CK$ ,  $C_a$  and  $C_b$ , and the size of MOS transistors  $M1 \sim M_r$ , and the clock frequency  $f$ .

The positive high-voltage generator becomes a negative voltage generator by replacing PMOS with NMOS, and by changing  $V_{DD}$  to GND. Figure 5 shows the schematic diagram of the new negative bias voltage

generator with 5-stages to obtain the low level gate signal  $V_{GL}$  (-10) of TFT. In the figure, the clock signals  $\bar{\phi}_1 \sim \bar{\phi}_4$  are in anti-phase with  $\phi_1 \sim \phi_4$  in Fig. 4. Also, the output voltage of the negative voltage generator with  $n$ -stages is approximately given by

$$V_o = -nV_{DD} + (n + 1)V_{DS} \quad (2)$$

Eqs. (1) and (2) show that the generators can provide various positive or negative voltages by simply changing the number of stages  $n$ .

### 3. Simulated Results

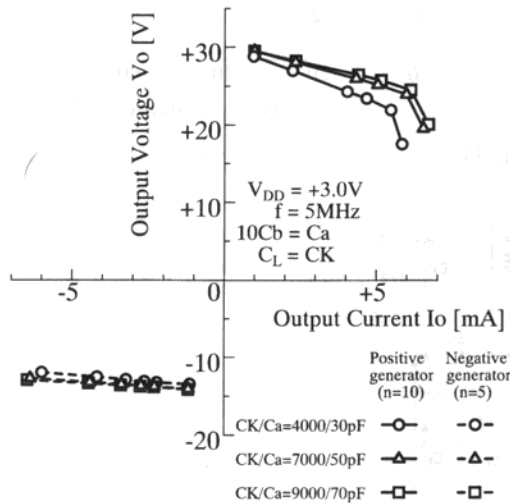
To verify the operation of the proposed generators, we carried out computer simulation by using HSPICE. Table 1 shows the device parameters of MOS-FETs for high-voltage process used for our simulation.

Figure 6 shows the output voltage  $V_o$  versus the output current  $I_o$  of the positive and negative generators for the different capacitance ratios  $CK/C_a$ . As can be seen in Fig. 6, when the output current is smaller than +5 mA, the positive generator with 10-stages shown in Fig. 3 generates voltages higher than +20 V. On the other hand, the negative voltage generator with 5-stages shown in Fig. 5 can generate the stable output voltage of about -12 V.

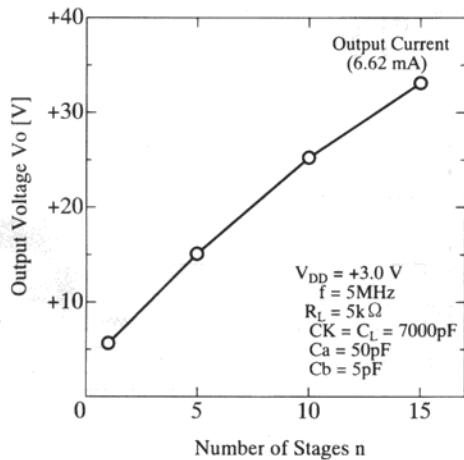
Figures 7 and 8, respectively, show dependence of the output voltage  $V_o$  of the positive high-voltage generator on the number of stages  $n$  (Fig. 7) and the supply voltage  $V_{DD}$  (Fig. 8). As shown in Fig. 7, the output voltage proportionally increases with the number

**Table 1** MOSFET device parameters.

Symbol	Parameter name	PMOS	NMOS	Units
$V_{TO}$	Zero-bias threshold voltage	-0.40	+0.40	V
$N_A$	Substrate doping	$1.0 \times 10^{16}$	$1.0 \times 10^{16}$	$\text{cm}^{-3}$
$t_{OX}$	Gate-oxide thickness	400	400	Å
$L$	Channel length	1.6	1.5	$\mu\text{m}$
$\lambda$	Channel-length modulation	0.02	0.02	$\text{V}^{-1}$
$\phi_s$	Surface inversion potential	0.70	0.70	V
$\mu_0$	Surface mobility	200	650	$\text{cm}^2/\text{V}\cdot\text{s}$
$\gamma$	Body-effect parameter	0.80	0.60	$\text{V}^{1/2}$



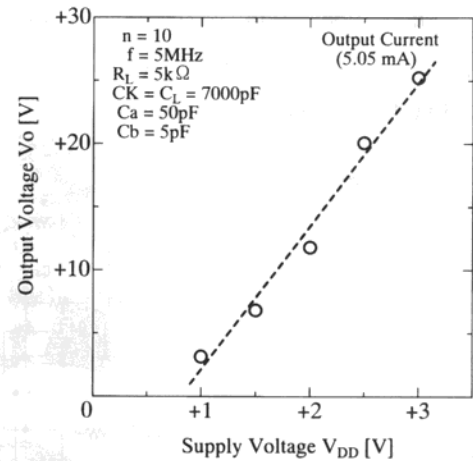
**Fig. 6** Output current vs. output voltage.



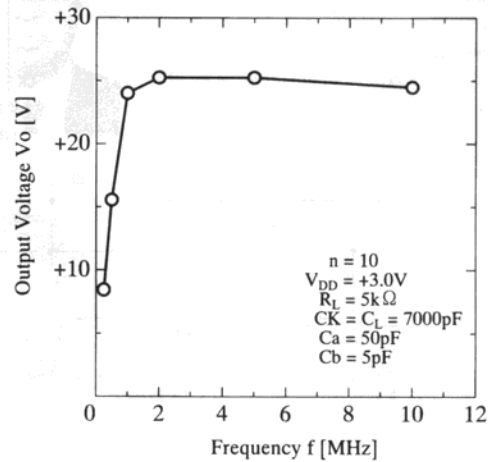
**Fig. 7** Number of stages vs. output voltage.

of stages  $n$ . Consequently, by varying the number of stages  $n$ , the generator can generate voltages having any amplitude. As shown in Fig. 8, the output voltage of the generator is nearly proportional to the supply voltage. Also, the generator can deliver the output current of about 5 mA to the load resistor when the output voltage is about +26 V.

Figure 9 shows the simulated output voltage  $V_o$  versus the clock frequency  $f$  of the positive 10-stage generator shown in Fig. 3. As shown in Fig. 9, the gen-



**Fig. 8** Supply voltage vs. output voltage.



**Fig. 9** Frequency vs. output voltage.

erator can generate the stable output voltage of about +26 V (the output current is about +5 mA) when the clock frequency is higher than 2 MHz.

Figure 10 shows the output voltage  $V_o$  versus the set-up time of the positive and negative generators for the different number of stages  $n$ . As can be seen in Fig. 10, to reach 90% of the maximum value of  $V_o$ , the positive generator with 10-stages takes about 46  $\mu\text{sec}$ . On the other hand, the negative generators with 5-stages and with 3-stages, respectively, take about 12  $\mu\text{sec}$  and 5  $\mu\text{sec}$ .

Figure 11 shows the output voltage  $V_o$  versus the

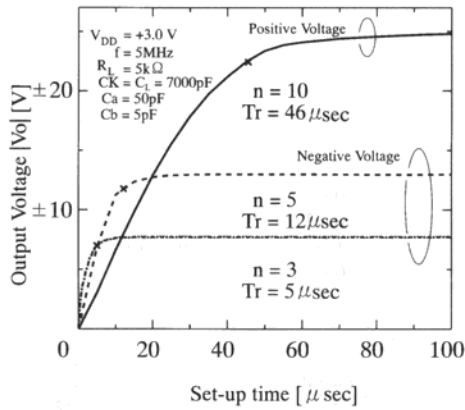


Fig. 10 Set-up time vs. output voltage.

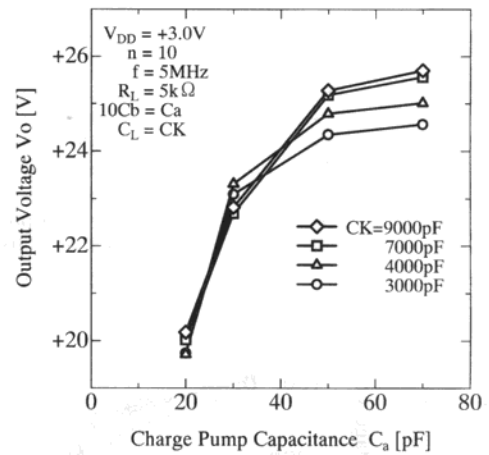


Fig. 11 Charge pump capacitance vs. output voltage.

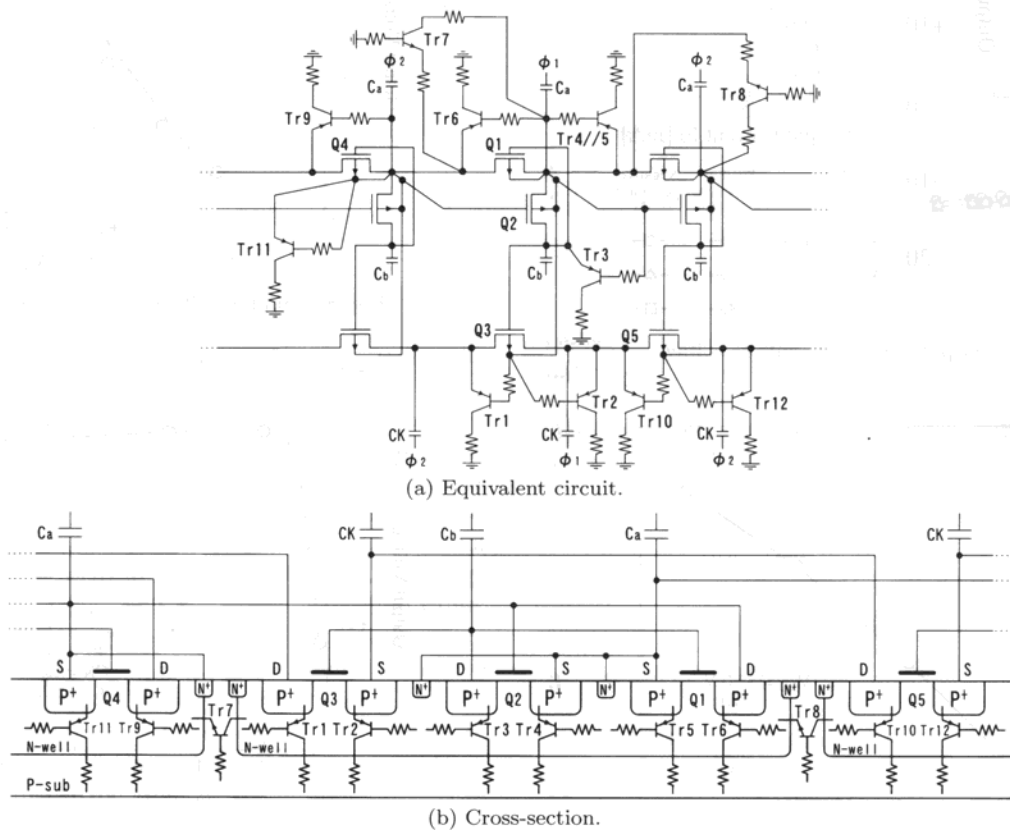


Fig. 12 A portion of positive generator including parasitic transistors.

charge pump capacitor  $C_a$  of the positive and negative generators for the different kick capacitor  $CK$ . As shown in Fig. 11, when the charge pump capacitor  $C_a$  is smaller than 35 pF, the output voltage under the conditions of  $CK$  are 3000 pF and 4000 pF is higher than the output voltage under the conditions of  $CK$  are 7000 pF and 9000 pF. On the other hand, when the charge pump capacitor  $C_a$  is larger than 35 pF, the output voltage under the conditions of  $CK$  are 7000 pF and 9000 pF is higher than the output voltage under the conditions of  $CK$  are 3000 pF and 4000 pF.

#### 4. Conclusion

We have proposed new positive and negative bias voltage generators for TFT-LCD's drivers utilizing charge pump circuits. Also, the operating characteristics of the proposed generators were examined by computer simulation (HSPICE) in detail. The generators can generate positive or negative voltages having various amplitude by simply changing the number of pumping stages. Also, the generators can be smaller size and be lower cost than the conventional DC-DC converters

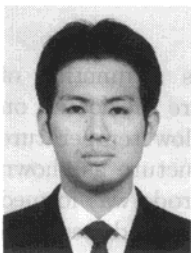
for TFT-LCD's drivers because can be designed without coils. Moreover, since coils are not included in the generators, it is possible to integrate the generators on a glass of TFT-LCD by using Poly-Si TFT-LCD technologies. In the integration of the proposed new bias generator, the equivalent circuit and the cross section of monolithic silicon chip can be illustrated as shown in Fig. 12. As can be find in Fig. 12, the some parasitic bipolar transistors exist at several node in the circuit. However, they do not operate in active mode because the bias voltages of these parasitic transistors are the reverse bias condition. In short, the proposed new generator for TFT-LCD's drivers is no problem for the parasitic devices.

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