

An Analog Sinusoidal Frequency-to-Voltage Converter

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Abstract—An analog sinusoidal frequency-to-voltage (F/V) converter, based on the use of nonlinear analog circuits, is introduced in this paper. The realization is composed of a differentiator, an integrator, and a translinear divider and square-rooter circuit. The proposed F/V converter can accurately and linearly convert a sinusoidal signal frequency into an output voltage, with fast response and low error, over more than two decades of frequency range. The method can also be implemented in monolithic integrated form.

I. INTRODUCTION

AN F/V converter is a device that generates an output voltage proportional to the frequency of an input signal. This device is very useful and has many applications in power system control, in processing of very-low-frequency signals, and in many fields of instrumentation. For example, it can be used as a frequency meter, as a control unit in a voltage-controlled oscillator (VCO), or as a frequency-measuring device in flowmeters and tachometer read outs in motor-speed controls. The basic requirements for a good F/V converter are low ripple, good linearity, fast response, and wide frequency range.

There are two fundamental approaches that can be employed to realize F/V converters [1]–[4]. The first approach is based on low-pass filtering of fixed duration pulses at a rate set by the input frequency. Most of the inexpensive F/V converters available commercially are ICS, such as the Analog Devices Models AD 451 and the AD 453, are operated in this mode. The second approach is based on counting the number of pulses over a given time interval. These conventional frequency-measuring techniques are unsuitable if the frequencies are low or if transient variations in frequency need to be detected. This is due to the fact that conventional F/V circuits involve a time-consuming averaging process. There are many methods especially designed for low-frequency operation [5]–[7]. However, their usefulness is limited to narrow frequency bands of operation. Further, an F/V converter can be achieved by using a voltage-to-frequency (V/F) converter, such as the Analog Devices multivibrator type V/F Model AD 537 or the charge-balance type V/F Model AD 650, in a phase-lock loop configuration. However, a

phase-locked loop is not generally used for precision F/V conversion because VCOs with adequate dynamic range and linearity have been hitherto unavailable.

Recently, many methods have been proposed for the frequency measurement of a purely sinusoidal signal [8]–[10]. The sinusoidal F/V converter has found application in communication systems. For example, it is useful in improving the transient response of automatic frequency control (AFC) of power systems or in measuring carrier frequency drift of RF signals after demodulation. All the published circuits perform analog or numerical computation on successive samples of the input signal, which is only suitable for a narrow range of input frequencies. In this paper, an alternative approach for realizing a sinusoidal F/V converter is described. The circuit performs mathematical operations using nonlinear analog circuits. The realization scheme is suitable for implementation in monolithic integrated form. Experimental results that demonstrate the accuracy, linearity, and fast response time of the converter are also included.

II. CIRCUIT DESCRIPTION

A. Basic Principle

Figure 1 shows the circuit diagram of the proposed F/V converter, which comprises three subcircuits, a differentiator, an integrator, and a combined divider and square-rooter circuit. Let us assume that the input signal V_{in} is a pure sinusoid having peak amplitude A , $V_{in} = A \sin(\omega t)$, and that the time constants of the differentiator and integrator circuits are τ_d and τ_i , respectively. Thus the output signals V_1 and V_2 of the integrator and differentiator circuits, respectively, can be written as

$$V_1 = (-A/\tau_i\omega) \cos(\omega t) \quad (1)$$

$$V_2 = (A\tau_d\omega) \cos(\omega t). \quad (2)$$

The absolute values of signals V_1 and V_2 , which can be achieved by the use of rectifier circuits, are fed into the divider and square-rooter circuit. Therefore, the output signal V_{OUT} can be given by

$$V_{OUT} = \sqrt{|V_2|/|V_1|} = \tau\omega \quad (3)$$

where $\tau = \sqrt{\tau_d \cdot \tau_i}$. We can see from (3) that the output V_{OUT} is a linear function of the input signal angular frequency ω , and is not dependent on the amplitude A of the input signal.

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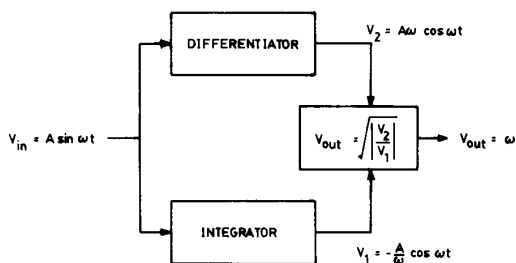


Fig. 1. Basic principle of the proposed F/V converter.

B. Translinear Divider and Square-Rooter Circuit

From the block diagram in Fig. 1, it is clear that the major part that produces the F/V action is the divider and square-rooter circuit. Usually, an operational amplifier (Op-amp) based circuit can be employed to construct the divider and square-rooter circuit [11]. However, in order that the proposed scheme can be implemented in a monolithic form, a translinear-principle based circuit will be described in this section. Consider the translinear circuit in Fig. 2, which is a single loop employing ten transistors. By assuming that the transistors of the transistor pairs (Q_i, Q'_i), where $i = 1, 3, 4, 6$, are perfectly matched and that the transistor's common emitter current gain $\beta = h_{FE} \gg 1$ or $\alpha \cong 1$, thus the base current $\cong 0$. Then the translinear principle gives [12]

$$I_{OUT} = I_4(I_2/I_1)^{1/2}. \quad (4)$$

We can see that the current I_{OUT} is in the form of the square root of the quotient ratio I_2/I_1 . Therefore, the translinear circuit in Fig. 2 provides a dividing and square rooting function.

The complete divider and square-rooter circuit is shown in Fig. 3. Op-amps A_1, A_2 and transistor Q_2 and op-amps A_3, A_4 and transistor Q_5 operate as full-wave rectifier circuits, converting the input voltages V_1 and V_2 into the currents I_2 and I_1 , respectively, where

$$I_2 = |(A\tau_d\omega) \cos(\omega t)| \quad (5)$$

$$I_1 = |(A/\tau_1\omega) \cos(\omega t)|. \quad (6)$$

By substituting (5) and (6) into (4), we get

$$I_{OUT} = I_4\tau\omega. \quad (7)$$

Then the output voltage

$$V_{OUT} = (R_L\tau I_4)\omega \quad (8)$$

which is a linear function of the input signal frequency, as is required.

C. Circuit Performance

For the translinear circuit, the major factors that contribute to the scaling errors or unwanted nonlinearities are due to the insufficiently high value of the current ampli-

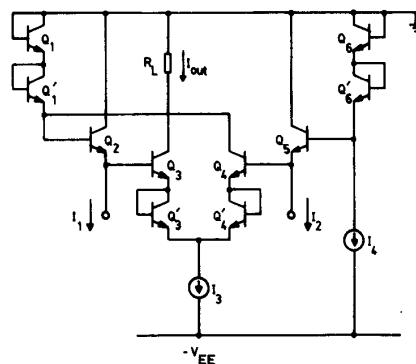


Fig. 2. A translinear divider and square-rooter circuit.

fication factor β and transistor mismatches. Transistors that are particularly closely matched with high values of β must be employed for Q_2 and Q_5 . This is because at low and very high frequencies the signal currents I_1 and I_2 , respectively, can be large. In such cases, the base currents of Q_2 and Q_5 cannot be neglected and will cause significant departure of I_{OUT} from the ideal value given in (4). The error due to transistor mismatching can be reduced by the adjustment of the gain of the rectifier stages.

In practice, owing to the inevitable presence of the offset current charging the integrating capacitor, a parallel resistor R_F is needed across the capacitor of the integrator circuit. Therefore the pole of the integrator circuit cannot be located exactly on the $j\omega$ axis. Moreover, in order to reduce amplification of the noise, whose frequency content may be well above the signal frequencies, by the differentiator, a resistor R_S is required to be connected in series with C_d . If a high value of R_F is needed in parallel with the integrating capacitor and, without loss of generality, if we let $\tau = \tau_i = \tau_d = R_i C_i$ be the integrator and differentiator time constants, then the effect of R_F upon the output voltage V_{OUT} can be written as

$$V_{OUT} = R_L I_4 \tau \omega \left\{ (1 + \epsilon^2 / \omega^2 \tau^2) / (1 + \omega^2 \tau_S^2) \right\}^{1/4} \cdot \{ \cos(\omega t) / \cos(\omega t + \gamma) \}^{1/2} \quad (9)$$

where $\tau_S = R_S C_d$, $\epsilon = R_i / R_F \ll 1$, and $\gamma = 90 - \tan^{-1}(\omega\tau/\epsilon)$ is a small angle, i.e. for $R_F = 1 \text{ M}\Omega$, $R_i = 2.2 \text{ k}\Omega$, $C_i = 0.1 \text{ }\mu\text{F}$ then $\gamma = 0.09^\circ$. For $\omega\tau_S^2 \ll 1$, we can see that the main effect is the introduction of a small distortion of the output-signal amplitude if R_F is large. For example, a conversion error of about 0.01% is expected if the signal frequency is 1 kHz, $R_L = 5 \text{ k}\Omega$, $R_S = 1 \text{ k}\Omega$, and $I_4 = 160 \text{ }\mu\text{A}$.

The other important sources of nonlinearities that will give rise to conversion errors in V_{OUT} are:

- The limited accuracies of the full-wave rectifier circuits.
- Temperature drift of the translinear circuit since it requires 10 matched transistors, which are not

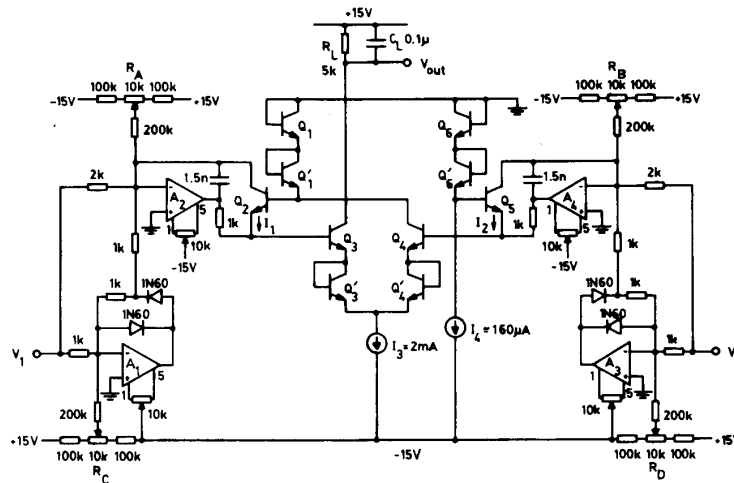


Fig. 3. Complete circuit diagram of the divider and square-rooter.

- available in a single integrated monolithic device (LM3046).
- Nonzero offset voltages of the integrator, differentiator, rectifiers and translinear circuits.
 - The offset signals from the outputs of the integrator and the differentiator will cause feedthrough of the fundamental to the output of the divider and square-rooter circuit as well as an increased DC offset voltage.
 - The dividing circuit will not be very accurate at both ends of the range, in particular, at very high frequency, when the output of the integrator or V_1 has a value of nearly zero, since the division by a very small quantity is not permissible with the divider.
 - We assume a pure sinusoidal input waveform in our mathematical computation and, therefore, harmonics and noise in the input waveform will cause error. This results in an increased level of noise at the output of the converter.

Error sources (c) through (f) result from the non-ideal characteristics of both the integrator and the differentiator circuits. Therefore, in order that the proposed F/V converter give a good performance in the required frequency range, special attention must be taken in the design of the integrator and the differentiator circuits.

The frequency response of the translinear circuit is high, i.e., of the order of 20 MHz [13], if the signals are in the form of currents. Therefore, the overall frequency response of the F/V circuit will be determined by the frequency response of the input circuits. The bandwidth of the F/V circuit will be primarily determined by the dynamic ranges and the noise levels of both the differentiator and integrator circuits. This is due to the fact that at very low frequency, i.e., $1/100$ of $1/\tau_d$, the differentiator output signal can become too low, while the in-

tegrator output signal can become saturated. At high frequencies, the reverse is also true.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

In this paper, differentiator and integrator circuits designed for the frequency range of 50 Hz to 5 kHz are employed to demonstrate the performance of the F/V circuit. As shown in Fig. 4, the integrator is designed for $V_{in} = 0.8 V_{peak}$, it provides $V_1 = 10 V_{peak}$ at 50 Hz, and $V_1 = 0.1 V_{peak}$ at 5 kHz. The differentiator part provides $V_2 = 50 mV_{peak}$ and $V_2 = 5 V_{peak}$ at 50 Hz and 5 kHz, respectively. The reason V_2 is set to $5 V_{peak}$, rather than to $10 V_{peak}$, at 5 kHz is to keep the current ratio (I_2/I_1) in (4) to a small value below 50 in order to reduce the non-linearity introduced by the translinear circuit.

The complete F/V circuit is constructed on a prototype board in order to experimentally demonstrate the performance of the converter. The op-amps employed are monolithic FET input op-amps LF 351's. The offset voltage of each amplifier is minimized to less than ± 0.2 mV. All n-p-n transistors, except Q_2 and Q_5 , are monolithic transistor arrays (LM3046), those that required close matching are contained in the same array package. Q_2 and Q_5 are in the form of supermatched pairs (LM394). All resistors used are $\pm 0.1\%$ tolerance resistors. Currents I_2 and I_4 are set to 2 mA and $160 \mu A$, respectively. The time constants of the integrator and the differentiator circuits, $\tau_i = R_i \cdot C_i$ and $\tau_d = R_d \cdot C_d$, are set to 2.2×10^{-4} and 2.0×10^{-4} s.

Resistors R_A and R_B in the circuit of Fig. 3 regulate the linearity of the converter. A procedure for adjusting the linearity of the divider and square-rooter circuit follows:

- Apply $V_{in} = 0.8 V_{peak}$ with a fixed frequency at 500 Hz and adjust the current I_4 so that $V_{OUT} \cong 500$ mV.
- Apply $V_{in} = 0.8 V_{peak}$ with a fixed frequency at 50 Hz and adjust R_B such that $V_{OUT} \cong 50$ mV.

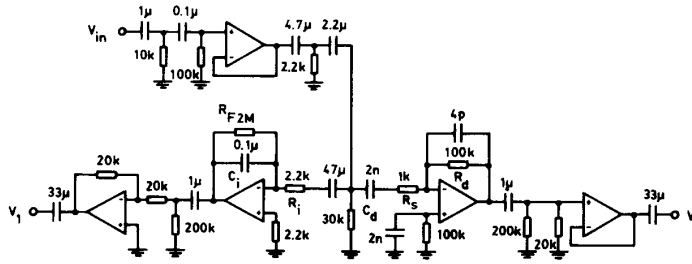


Fig. 4. The differentiator and integrator circuits designed for the frequency range from 50 Hz to 5 kHz.

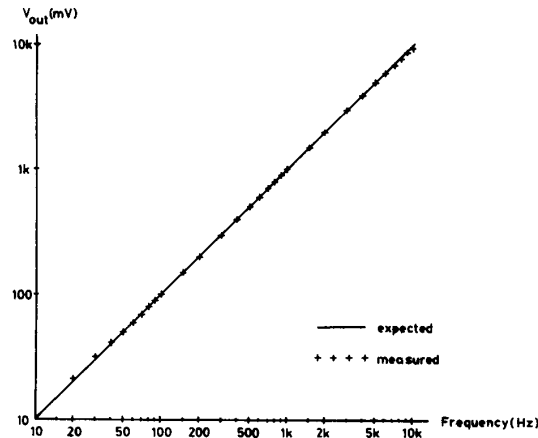


Fig. 5. Plot of V_{OUT} against frequency.

- c) Apply $V_{in} = 0.8 V_{peak}$ with the fixed frequency at 5 kHz and adjust R_A such that $V_{OUT} \cong 5$ V.
- d) Repeat steps (a) through (c) until the measured V_{OUT} errors from steps (a), (b), and (c) are less than $\pm 1\%$.

Fig. 5 shows the plot of the measured output voltage V_{OUT} against the input signal frequency, where the amplitude of the input signal is kept constant at $V_{in} = 0.8 V_{peak}$. It is clearly seen that the experimental results agree very well with the calculated values over more than two decades of the frequency range. The measured V_{OUT} error does not exceed $\pm 0.5\%$, where the error is found to be less than 0.1% in the frequency range of 400 Hz to 5 kHz and less than 0.5% in the frequency range of 50–300 Hz. As already discussed in this section, the bandwidth of the F/V circuit is determined by the dynamic ranges of both the integrator and the differentiator circuits. Therefore, for a specific application of the F/V converter, the integrator and the differentiator circuits must be redesigned in order to work in the required frequency range.

Experimental results which illustrate the fast response to a sudden frequency change of the input frequency are shown in Fig. 6. The circuit response is measured as follows: An input signal is applied to a VCO to obtain a frequency-modulated (FM) signal. The FM signal is then

fed into the proposed F/V converter and the V_{OUT} is monitored in order to compare with the input signal of the VCO. Fig. 6(a) shows the response of the V_{OUT} to step changes in the input frequency from 50–500 Hz and vice versa. We can see that the measured V_{OUT} (lower trace) can follow the square-wave input signal of the VCO (upper trace) with 2-ms time delay and 10-mV ripple. Fig. 6(b) shows that the conversion circuit can lock to the input frequency within a fraction of a cycle. In contrast, the conversion time for the AD 537 in a phase-lock configuration requires three or four cycles [14]. Fig. 6(c) shows the test that is conducted by continuously sweeping the input frequency in the range from 50 Hz to 5 kHz. The result demonstrates the accuracy of better than 0.1% and the measured nonlinearity at 99% dynamic range is less than $\pm 0.5\%$. However, it should be noted that the linearity and accuracy performance depend strongly on the type of VCO that is used. In addition, it is expected that the circuit in an actual integrated form will have a much better performance than the performance measured from the bread-boarded circuit.

IV. CONCLUSION

In this paper, we have demonstrated the use of a nonlinear analog circuit technique to realize a sinusoidal F/V

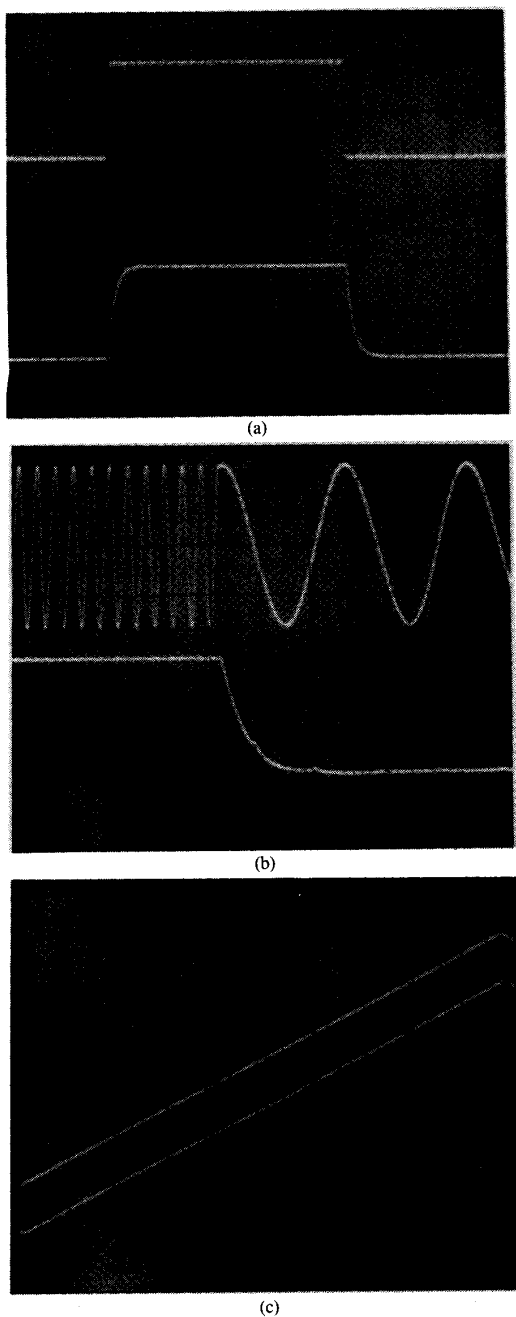


Fig. 6. Response time of the converter. (a) Response to a step change of frequency. (upper trace: 0.2 V/div; lower trace: 1 V/div; horizontal scale: 5 ms/div). (b) Response to a step change of frequency of an input signal. (upper trace: 0.5 V/div; lower trace: 0.5 V/div; horizontal scale: 2 ms/div). (c) Response to a continuous sweeping of frequency. (upper trace: 0.2 V/div; lower trace: 1 V/div; horizontal scale: 20 ms/div).

converter. Since the computation is performed through an analog operation, the converter has a fast response time to frequency changes. The performance of the F/V converter for the frequency range from 50 Hz to 5 kHz has been presented. Experimental results showing the linear F/V characteristic, the rapid step response and the low ripple are given. It should be noted that, for applications that require simultaneous detection of both amplitude and frequency the proposed F/V can easily be combined with the peak amplitude detection scheme discussed in [15].

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